

ELECTRONIC INFORMATION DISCLOSURE STATEMENT

Electronic Version v18

Stylesheet Version v18.0

Title of Invention

Reducing Coupling Effect on Reference Voltages When Output Buffers Implemented with Low Voltage Transistors Generate High Voltage Output Signals

Application Number :

10 710 874

Confirmation Number:

First Named Applicant:

Rajat CHAUHAN

Attorney Docket Number:

TI-38154

Art Unit:

Examiner:

Search string:

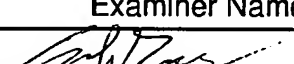
(4704547).pn

US Patent Documents

Note: Applicant is not required to submit a paper copy of cited US Patent Documents

init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass
AT	1	4704547	1987-11-03	Kirsch			

Signature

Examiner Name	Date
	2/17/06

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Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Complete if Known

Application Number	10/710874
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Filing Date	August 10, 2004
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First Named Inventor	Rajat Chauhan
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Group Art Unit	UNASSIGNED
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Examiner Name	UNASSIGNED
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Attorney Docket Number TI-38154

U.S. PATENT DOCUMENTS

[illegible]

FOREIGN PATENT DOCUMENTS

[illegible]

**Examiner
Signature**

Date Considered

2/17/00

*EXAMINER: Initial reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ Unique citation designation number. ² See attached Kinds of U.S. Patent Documents. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**AUG 20 2004
U.S. PATENT AND TRADEMARK OFFICE
(Use as many sheets as necessary)**Complete if Known**

Application Number	10/710874
Filing Date	August 10, 2004
First Named Inventor	Rajat Chauhan
Group Art Unit	UNASSIGNED
Examiner Name	UNASSIGNED
Attorney Docket Number	TI-38154

2 of 2

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
AT		HECTOR SANCHEZ, JOSHUA SIEGEL, CARMINE NICOLETTA, JAMES J.P AND NISSEN, JOSE ALVAREZ, "A Versatile 3.3V/2.5V/1.8-V CMOS I/O Driver Built in a 0.2-um, 3.5nm Tox, 1.8-V CMOS Technology" In IEEE J. Solid State Circuits Vol 34, pp. 1501-1511, No. 11, November 1999.	
AT		CHANGSIK YOO, MIN-KYU KIM, AND WONCHANG KIM, "A Static Power Saving TTL-to -CMOS Input buffer" in IEEE Journal of Solid State Circuits. Vol 30, pp. 616- 620, No. 5, may 1995.	

Examiner
SignatureDate
Considered

2/17/06

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